UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,621	08/06/2003	Hsi-Kuei Cheng	TSM02-0971	8481

43859 7590 02/24/2005

SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
NGUYEN, HA T	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/635,621	CHENG ET AL.	
	Examiner	Art Unit	
	Ha T. Nguyen	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notice to applicant

1. Applicants' Amendment and Response to the Office Action mailed 11-18-4 and Request for a Continued Examination have been entered and made of record. Following is an Office Action responding to the request.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

3. Claims 12-13 and 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cave et al. (USPN 6313024, hereinafter "Cave") in view of Mehta et al. (USPN 6261944, hereinafter "Mehta").

Referring to Figs. 1-8 and related text, Cave discloses [Re claim 34] a method of forming post passivation interconnects for an integrated circuits the method comprising: forming a passivation layer 75-85 over a substantially complete integrated circuit and over a first plurality of contact pads 40, the first plurality of contact pads being in a first connection pattern, wherein the passivation layer is formed from a non-oxide material; forming an oxide buffer layer 86 over and abutting the passivation layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the passivation layer; forming a metal layer 88 over the oxide buffer layer; and patterning the metal layer to form a second connection pattern comprising a second plurality of contact pads (see par. bridging cols. 7-8), wherein the second connection pattern differ from the first connection pattern. But it does not disclose expressly wherein at least some of the second plurality of contact pads are electrically connected to at least some of the first plurality of contact pads. However, the missing limitation is well known in the art because Mehta discloses this feature (See Fig. 5, # 49). A person of ordinary skill is motivated to modify Cave with Mehta to obtain shorter wiring to external devices .

[Re claims 12-13] Cave fails to disclose wherein forming an oxide buffer layer comprises forming an oxide buffer layer with a thickness of less than 25 nanometers; wherein thickness of the nitride passivation layer is at least about 20 times greater than the thickness of the oxide

buffer layer. However any variation in thickness in the present claims is obvious in light of the cited art, because the changes in thickness produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the art. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. In re Aller, Lacey and Hall, 105 U.S.P.Q. 233, 235. In re Reese 129 U.S.P.Q. 402, 406.

Therefore, it would have been obvious to combine Cave with Mehta to obtain the invention as specified in claims 12-13 and 34.

4. Claims 22-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cave in view of Saito et al. (USPAP 20010045651, hereinafter "Saito").

[Re claim 22] Cave also discloses a method of forming a semiconductor device, the method comprising: providing a silicon substrate having a plurality of active devices formed therein, the active devices being interconnected by a plurality of metal layer including an uppermost metal layer, the uppermost metal layer including a first plurality of contact pads 40; forming a nitride passivation layer overlying the uppermost metal layer; forming an oxide buffer layer overlying the nitride passivation layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the nitride passivation layer; and forming a post passivation metal layer overlying the oxide buffer layer, the post passivation metal layer being patterned (See par. bridging cols. 7 and 8). But it fails to disclose expressly the first plurality of contact pads could otherwise be used to provide electrical connection to an external component in packaging an integrated circuit chip comprising the semiconductor device by forming wire bonds or solder balls on the first plurality of contact pads; and passivation layer overlying the uppermost metal layer except for selected contact openings to the first plurality of contact pads , and the post passivation metal layer are patterned to electrically couple the first plurality of contact pad to a second plurality of contact pads formed in the post passivation metal layer. However the missing limitations are well known in the art because Saito discloses these features (see Fig. 12, # 43, 47). It would have been obvious to a person of ordinary skills in the art to modify Cave with Saito to make short connections between the first contact pads and external devices.

[Re claim 23] Cave also discloses wherein forming a nitride passivation layer comprises forming a silicon nitride layer and wherein forming an oxide buffer layer comprises forming a silicon oxide layer (See par. bridging cols. 7 and 8) ; and

[Re claim 28] wherein the uppermost metal layer comprises a layer of copper (see par. bridging cols. 2-3 or 6-7).

[Re claims 24-25] Cave fails to disclose wherein forming an oxide buffer layer comprises forming an oxide buffer layer with a thickness of less than 25 nanometers; wherein thickness of the nitride passivation layer is at least about 20 times greater than the thickness of the oxide buffer layer. However any variation in thickness in the present claims is obvious in light of the cited art, because the changes in thickness produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the art. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. In re Aller, Lacey and Hall, 105 U.S.P.Q. 233, 235. In re Reese 129 U.S.P.Q. 402, 406.

[Claim 26] Cave also discloses wherein the uppermost metal layer includes a plurality of contact regions disposed around the periphery of the chip and the contact pads are arranged over a central portion of the semiconductor chip (see Fig. 9 and related text).

Therefore, it would have been obvious to combine Cave with Saito to obtain the invention as specified in claims 22-26 and 28.

5. Claims 1 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cave in view of Saito, as applied above, and further in view of Mehta.

[Re claim 1] The combined teaching of Cave and Saito discloses substantially the limitations of claim 1, as shown above. It also discloses forming a second plurality of contact pads while forming the second connection pattern and as part of the second connection pattern (see Fig. 12). But the combined teaching of Cave and Saito fails to disclose expressly the step of removing a top portion of the buffer layer. However, the missing limitation is well known in the art because Mehta discloses this feature (See col. 5, lines 22-53). A person of ordinary skill is motivated to modify Cave and Saito with Mehta to obtain device of planar surface for ease of

formation of subsequent layers of uniform thickness ensuring better control of device quality and reliability.

[Re claims 6-7] Cave also discloses wherein the passivation layer comprises a layer of silicon nitride and wherein the passivation layer comprises more than one layer and wherein an uppermost layer comprises silicon nitride (see par. bridging cols. 7-8).

[Re claims 8-9] Arguments used for the rejection of claims 12-13 and 24-25 also apply.

Therefore, it would have been obvious to combine Cave and Saito with Mehta to obtain the invention as specified in claims 1, 6-7, and 8-9.

6. Claims 2-5, 11, and 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cave in view of Mehta, Saito, or Saito and Mehta, as applied above, and further in view of Fan (USPN 6022809).

The combined teaching of Cave and the applied references discloses substantially the limitations of claims 2-5, 11, and 29-33, as shown above. But it fails to disclose expressly wherein the top portion of the buffer layer is removed in a cleaning chamber having an inner wall comprising primarily quartz; wherein the cleaning chamber is in a vacuum condition during the removing step and wherein the post passivation metal layer is deposited over the buffer layer after the removing step without breaking the vacuum condition in the cleaning chamber; wherein passivation layer is formed in a first chamber that is in a vacuum condition and wherein the buffer layer is formed over the passivation layer in the fist chamber and without breaking the vacuum condition in the first chamber after forming the passivation layer; wherein the top portion of the buffer layer is removed in the first chamber, the method further comprising breaking a vacuum condition in the first chamber before the step of etching the buffer layer. However, the missing limitations are well known in the art because Fan discloses that a vacuum chamber having inner walls of primarily quartz is used to etch material (See par. bridging cols. 5 and 6). A person of ordinary skill is motivated to modify Cave and the applied references with Fan to obtain device containing less contaminants ensuring better quality. The combination of the applied references does not expressly disclose the details about the vacuum condition in etching and depositing different layers. However it would have been obvious for a person of ordinary skills in the art to use one or a suitable number of chambers to etch and deposit different

materials to meet the availability of equipment and the requirements in cost and quality of the devices made.

Therefore, it would have been obvious to combine Cave and the applied references with Fan to obtain the invention as specified in claims 2-5, 11, and 29-33.

7. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cave in view of Saito, as applied above, and further in view of Carey et al. (USPN, hereinafter "Carey").

The combined teaching of Cave and Saito discloses substantially the limitations of claim 27, as shown above.

But it fails to disclose expressly providing a package substrate having a plurality of contact pads arranged in a configuration corresponding to the contact pads on the semiconductor chip; and attaching the contact pads of the package substrate to the contact pads on the semiconductor chip via a plurality of solder bumps, wherein the solder bumps electrically couple the contact pads on the semiconductor chip with the contact pads on the package substrate.

However, it is well known in the art because Carey discloses this feature (See fig. 1).

A person of ordinary skill is motivated to modify Cave and Saito with Carey to connect a chip to a carrier substrate.

Therefore, it would have been obvious to combine Cave and Saito with Carey to obtain the invention as specified in claim 27.

Response to Amendment

8. In view of Applicants' cancellation of claim 10, the rejection of claim 10 has been rendered moot.

In view of Applicants' arguments and amendment to the claims, the rejections of claims 1-9 and 11-33, as stated in the Office Action mailed 11-18-4 have been withdrawn.

Applicants' arguments concerning the rejections have been rendered moot in view of the new ground of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha T. Nguyen whose telephone number is (571) 272-1678. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week. The telephone number for Wednesday is (703) 560-0528.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ha Nguyen
Primary Examiner
2- 21- 05